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10/784,782	02/24/2004	Jung Gwan Han	YHK-0132	2202

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,782	HAN ET AL.	
	Examiner	Art Unit	
	STEPHEN G. SHERMAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-14,16 and 19-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14,16 and 19-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 30 July 2008. Claims 1-6, 8-14, 16 and 19-28 are pending.

Response to Arguments

2. Applicant's arguments filed 30 July 2008 have been fully considered but they are not persuasive.

On page 10 of the response the applicant agues that the applied references do not teach or suggest the features of claim 1. Specifically the applicant argues that in paragraph [0065] Akiba chooses cells to be lit by applying a positive pulse in synchronization with applying a negative address pulse, and then chooses cells not to be lit by applying a voltage at a same timing that a scan pulse is maintained at zero. The applicant then argues that Higashino discloses that on-cells are selected by discharge and off-cells are selected by no discharge, and thus the combination of the references does not result in a positive pulse being used as a third voltage to select the off-cells. The examiner respectfully disagrees.

While the examiner agrees with what the applicant states paragraph [0065] of Akiba describes, the examiner used paragraph [0067] in the rejection, which states that what is shown in the Figures and described in paragraph [0065] can essentially be reversed i.e. the off-cells could be "chosen" instead of the on-cells. Akiba as only used

for its teaching of selecting off-cells instead of selecting on-cells. Akiba was never meant to be bodily incorporated into Higashino. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Akiba suggests to selected off-cells instead of on-cells in paragraph [0067], and as described in the rejection, it would have been obvious to use the idea of selecting off-cells using a voltage instead of selecting on-cells using a voltage as taught by Akiba in the plasma display device taught by Higashino et al. in order to yield the predictable result of selecting the cells. Thus the rejection is proper.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 8, 9, 13, 16 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashino et al. (US 2003/0020674) in view of Akiba (US 2003/0122742).

Regarding claim 1, Higashino et al. disclose a plasma display having an address electrode, a scan electrode and a sustain electrode, wherein cells are arranged at intersections of the electrodes (Figures 5-7 show the scan electrode as the Second Display Electrode I, the sustain electrode as the First display Electrode i and the address electrode as the Address Electrode i.), comprising:

a first driver for initializing the cells (Figure 7 shows the Scn2 Drive 303, where Figure 5 shows that there are initialization periods T1 and T2.);

a second driver (Figure 7 shows a second driver Scn1 Drive 302.); and

an address driver to select on-cells and to select off-cells (Figure 7 shows Data Drive 304.),

wherein on-cells are selected by the address driver applying data of a first voltage to the address electrode and the first driver applying a scan pulse of a second

voltage to the scan electrode (Figure 5 shows that on-cells are selected by the address driver shown in Figure 7 using data of a first voltage PaA while the first driver shown in Figure 7 applies a scan pulse PaS2 to the scan electrode.), and

off-cells are selected by the address driver applying data of a third voltage to the address electrode in synchronism with the scan pulse of the second voltage (Figure 5 shows that off-cells are selected by the address driver in Figure 7 using 0 or a ground voltage while the first driver shown in Figure 7 applies a scan pulse PaS2 to the scan electrode.),

wherein the second voltage is a positive voltage (Figure 5 shows that PaS2 is a positive voltage.).

Higashino et al. fail to teach wherein the third voltage is greater than the first voltage, and wherein the first voltage to select the on-cells is one of zero voltage and a ground voltage GND.

Akiba discloses a plasma display where choosing lit cells can be done using a voltage while un-lit cells can be chosen using a ground voltage (Paragraphs [0065]-[0066]). Akiba then discloses that although the cells to be lit can be chosen using a voltage, it is possible to reverse this and choose the cells not to be lit, i.e. off-cells, using a voltage (Paragraph [0067]). Applying this concept to Higashino et al. would result in the positive pulse PaA being used as the third voltage to select the off-cells while 0 or ground would be used as the first voltage to select on-cells, meaning that the third voltage would be greater than the first voltage.

Therefore, since Higashino et al. and Akiba both teach methods for selecting on and off cells for a plasma display, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the idea of selecting off-cells using a voltage instead of selecting on-cells using a voltage as taught by Akiba in the plasma display device taught by Higashino et al. in order to yield the predictable result of selecting the cells.

Regarding claim 8, Higashino et al. and Akiba disclose the plasma display of claim 1.

Higashino et al. also disclose wherein the first driver and the second driver alternately apply a sustain pulse of a fourth voltage to the scan electrode and the sustain electrode to cause a sustain discharge with respect to the on-cells (Figure 5 shows that the drivers 302 and 303 shown in Figure 7 will alternately supply the sustain voltage Vsus to the scan and sustain electrodes.).

Regarding claim 9, please refer to the rejection of claim 1, and furthermore Higashino et al. also disclose wherein the second voltage is higher than the first voltage (As explained above, the first voltage is 0, while the second voltage PaS2, i.e. scan voltage, is a positive value, meaning that the second voltage is higher than the first.).

Regarding claim 13, Higashino et al. and Akiba disclose the method of claim 9.

Higashino et al. also disclose the method further comprising supplying a fourth voltage to the sustain electrode to select the on-cells and the off-cells, in an address period (Figure 5 shows that a voltage of PaS1 is applied to the sustain electrode in the address period to selected the cells.).

Regarding claim 16, this claim is rejected under the same rationale as claim 8.

Regarding claim 19, Higashino et al. and Akiba disclose the plasma display of claim 1.

Higashino et al. also disclose wherein the address driver applies data of the first voltage to the address electrode during a reset period (Figure 5 shows initialization periods T1 and T2, i.e. reset period, where the address electrode is at ground.) and applies data of the third voltage to the address electrode during an address period (Figure 5 shows that PaA is applied during the address period T3.), and the first driver applies the scan pulses to the scan electrode during the address period (Figure 5 shows that the scan pulses PaS2 are applied during the address period T3.).

Regarding claim 20, Higashino et al. and Akiba disclose the method of claim 9.

Higashino et al. also disclose wherein the scan pulse of the second voltage to select on-cells is applied during an address period and the scan pulse to select off-cells is applied during the address period (Figure 5 shows that the scan pulses are all applied during the address period T3.).

Regarding claim 21, Higashino et al. and Akiba disclose the method of claim 1.

Higashino et al. also disclose the method further comprising creating an address discharge within the selected on-cells when a subsequent sustain voltage is applied during a sustain period (Figure 5 shows sustain pulses Vsus which cause address discharge within on-cells during sustain period T4.).

Regarding claim 22, Higashino et al. and Akiba disclose the method of claim 21.

Higashino et al. also disclose wherein creating the address discharge includes avoiding an address discharge within the selected off-cells during the sustain period (Inherently, if a cell is off, address discharge will not occur, i.e. will be avoided.).

Regarding claim 23, Higashino et al. and Akiba disclose the method of claim 9.

Higashino et al. also disclose the method further comprising maintaining wall charges within the selected off-cells during a sustain period (Paragraphs [0094]-[0095] explain that the sustain voltage is maintained so that discharge only occurs in cells written, and not in off-cells meaning that the wall charges are not erased, but rather that the voltage applied is not enough to cause discharge.).

Regarding claim 24, Higashino et al. and Akiba disclose the method of claim 23.

Higashino et al. also disclose wherein selecting the on-cells and selecting the off-cells occurs during an address period preceding the sustain period (Figure 5 shows that the cells are selected during the address period.).

6. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashino et al. (US 2003/0020674) in view of Akiba (US 2003/0122742) and further in view of Du et al. (US 2003/0071577).

Regarding claim 2, Higashino et al. and Akiba disclose the plasma display of claim 1.

Higashino et al. and Akiba fail to teach wherein the first driver supplies a waveform to the scan electrode and the second driver applies an identical waveform to the sustain electrode sustain electrode.

Du et al. disclose wherein drivers of a plasma display supplies an identical waveform to both of the scan electrode and the sustain electrode (Figure 3 shows the reset period T1, in which PY1 is applied to the scan electrode Y and PX2 is applied to the sustain electrode X, where PY1 is identical to PX2.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to apply an identical waveform to both the sustain and scan electrodes as taught by Du et al. with the plasma display taught by the combination of Higashino et al. and Akiba in order to provide a plasma display in which the distribution of wall charges in the pixel units in the reset period are made to be less different.

Regarding claim 10, this claim is rejected under the same rationale as claim 2.

7. Claims 3, 6, 11, 14 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashino et al. (US 2003/0020674) in view of Akiba (US 2003/0122742) and further in view of Du et al. (US 2003/0071577) and Mizobata (US 2003/0095084).

Regarding claim 3, Higashino et al., Akiba and Du et al. disclose the plasma display of claim 2.

Higashino et al., Akiba and Du et al. fail to teach wherein the initializing driver simultaneously supplies a falling ramp waveform and a rising ramp waveform following the falling ramp waveform to the scan electrode and the sustain electrode.

Mizobata et al. disclose a plasma display wherein an initializing driver supplies a falling ramp waveform and a rising ramp waveform following the falling ramp waveform to the scan electrodes (Figure 3 shows that during period 7, there is a falling ramp supplied to the electrodes S1 to Sm during period 2 and that there is a rising ramp supplied to the electrodes S1 to Sm following the falling ramp in period 3.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the waveforms taught by the combination of Higashino et al., Akiba and Du et al. have the falling and rising ramp structure as taught by Mizobata et al. in order to improve the darkroom contrast ratio.

Regarding claim 6, Higashino et al., Akiba, Du et al. and Mizobata et al. disclose the plasma display of claim 3.

Du et al. also discloses wherein the falling ramp waveform decreases from a first negative voltage to a second negative voltage, an absolute value of the second negative voltage being greater than an absolute value of the first negative voltage and wherein the rising ramp waveform increases from the first negative voltage to zero voltage (Figure 7 shows pulse PY2 applied to the scan electrode Y. In this waveform, the lowest voltage is the second voltage and the voltage at which the waveform begins to fall is the first voltage, making the second voltage larger than the first. Figure 7 also shows that the rising part of the waveform PY2 is from the second voltage to a ground potential.).

Regarding claim 11, this claim is rejected under the same rationale as claim 3.

Regarding claim 14, this claim is rejected under the same rationale as claim 6.

Regarding claim 25, this claim is rejected under the same rationale as claim 3.

Regarding claim 26, this claim is rejected under the same rationale as claim 3.

8. Claims 4-5, 12 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashino et al. (US 2003/0020674) in view of Akiba (US

2003/0122742) and further in view of Mizobata (US 2003/0095084) and Kobayashi (US 6,876,340).

Regarding claim 4, Higashino et al. and Akiba disclose the plasma display of claim 1.

Higashino et al. and Akiba fail to teach wherein the initializing driver supplies a falling ramp waveform and a rising ramp waveform following the falling ramp waveform to the scan electrode, and the second driver supplies a fourth voltage to the sustain electrode.

Mizobata discloses a plasma display wherein an initializing driver supplies a falling ramp waveform and a rising ramp waveform following the falling ramp waveform to the scan electrodes (Figure 3 shows that during period 7, there is a falling ramp supplied to the electrodes S1 to Sm during period 2 and that there is a rising ramp supplied to the electrodes S1 to Sm following the falling ramp in period 3.), and supplies a fourth voltage to the sustain electrode (Figure 3, lines C1-Cm receive a voltage during period 7.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the waveforms taught by the combination of Higashino et al. and Akiba have the falling and rising ramp structure as taught by Mizobata et al. in order to improve the darkroom contrast ratio.

Higashino et al., Akiba and Mizobata fail to teach wherein the fourth voltage is a negative voltage.

Kobayashi discloses a plasma display in which a negative voltage is applied to the sustain electrodes during a reset period (Figure 7, electrodes Y1-Yn have a voltage that goes below 0 applied, i.e. a negative voltage.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use make the voltage applied to the sustain electrode as taught by the combination of Higashino et al., Akiba and Mizobata have a negative voltage as taught by Kobayashi in order to provide a plasma display in which the distribution of wall charges in the pixel units in the reset period are made to be less different.

Regarding claim 5, Higashino et al., Akiba, Mizobata and Kobayashi disclose the plasma display of claim 4.

Kobayashi also discloses wherein the second driver comprises a sustain driver for supplying the fourth voltage to the sustain electrode in an address period to select on-cells and the off-cells (Figure 7 shows the voltage being applied to the sustain electrode during the address period.).

Regarding claim 12, this claim is rejected under the same rationale as claim 4.

Regarding claim 27, this claim is rejected under the same rationale as claim 4.

Regarding claim 28, this claim is rejected under the same rationale as claim 4.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN G. SHERMAN whose telephone number is (571)272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen G Sherman/
Examiner, Art Unit 2629

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

8 September 2008